

**REMARKS**

In section 3 of the Office Action, the Examiner applied the Litwin patent.

In Figure 1, the Litwin patent discloses a varactor 10 comprising a p-MOS enhancement transistor formed in a p type silicon substrate 11. An n type well 12 is formed in the p-type silicon substrate 11, and a p+ type source region 13 and a p+ type drain region 14 are formed in the n type well 12. An insulating layer 15 is formed over the p type silicon substrate 11, the n type well 12, the p+ type source region 13, and the p+ type drain region 14. A poly-silicon gate 16 is formed on the insulating layer 15 covering at least a part of the n type well 12 such that the gate 16 is electrically insulated from the n type well 12. A first electrode C<sub>A</sub> is commonly connected to both the source region 13 and to the drain region 14, and a second electrode C<sub>B</sub> is connected to the gate 16.

A varactor 20 is similarly constructed except that the source and drain regions are n+ type and the well is p type, and a varactor 30 is also similarly constructed except that the source and drain regions are n+ type and the well is n type.

The gate length  $L_g$  (corresponding to the distance between the source and drain regions) is less than 2 microns, and the gate width  $W_g$  is less than 20 microns.

Figures 7-13 illustrates composite varactors 70 and 80 having an n type well regions and p+ type source and drain regions. Gates are separated from the varactor substrate and the well regions by an insulating layer. The gates forms a first electrode of the composite varactor, and the p+ type regions are connected to a second electrode of the composite varactor.

The composite varactors disclosed in the Litwin patent are thus made up of a number of MOS transistors, each having a source region, a drain region, a gate, and a channel region formed between the source region and the drain region. These MOS transistors are coupled in parallel to form the composite varactor. The composite varactor can be provided with a high Q factor by using small dimensions of the gate and the channel region and by keeping the resistance of the gate (and its connection) as small as possible. Small dimensions of the gate and the channel region give rise to a varactor having a capacitance with a sometimes unacceptable small numerical value. However, a suitable capacitance can be

achieved by coupling a suitable number of varactors in parallel. Composite varactors having high Q factors and suitable capacitances are thereby provided and may be used in high frequency applications.

In section 4 of the Office Action, the Examiner added the Chiang patent and the Tsang patent to the Litwin patent.

The Chiang patent discloses a thin film polysilicon varactor which has a larger effective gate area in accumulation than in depletion.

The Tsang patent, in Figures 1 and 2, discloses a conventional NMOS transistor 10 having a P- well 12, an n+ drain region 16, a p+ well region 18, and an n+ source region 20 formed in the P- well 12. The conventional NMOS transistor 10 has a parasitic npn transistor 26.

The Tsang patent, in Figures 3 and 4, discloses a CMOS output transistor circuit having an NMOS transistor 28 and a PMOS transistor 30. The NMOS transistor 28 consists of a P- well 32, an n+ drain region 34, an n+ source region 36, a p+ well region 38, and a gate 40 formed on an insulating layer 42. The PMOS transistor 30 has an n- well 44, a p+ drain region 46, a p+ source region 48, an n+ well region 50, and a gate 52 provided on top of an insulating layer 54. The CMOS

output transistor circuit includes parasitic thyristors 56 and 58.

The Tsang patent, in Figures 5 and 6, discloses an NMOSFET output stage transistor 60 having a P- well region 62, a source region 64, an N+ drain region 66, a gate 68 deposited on an insulating layer 70, and a P region 72. The source region 64 has alternating N+ and P+ sub-regions 76 and 78.

The Tsang patent, in Figures 7 and 8, discloses a PMOSFET output stage transistor 80 having an N- well 82, a source region 84, a P+ drain region 86, a gate 88, and an N region 90. The source region 84 has alternating P+ and N+ sub-regions 94 and 96.

Newly added independent claim 32 is directed to a method of making a varactor in which a plurality of alternating P- wells and N+ regions are formed in a silicon layer of an SOI structure such that the P- wells form N+/P- junctions with the N+ regions, and such that each of the P- wells and the N+ regions extends completely through the silicon layer to an insulation layer of the SOI structure. Each of a plurality of gate oxides is formed above a corresponding one of the P- wells, and each of a plurality of silicon gates is formed above a corresponding one of the gate oxides. The

silicon gates are electrically coupled together, and the N+ regions are electrically coupled together.

The Litwin patent, the Chiang patent, and the Tsang patent do not disclose making a varactor so that alternating P- wells and N+ regions are formed in a silicon layer of an SOI structure such that each of the P- wells and the N+ regions extends completely through the silicon layer to an insulation layer of the SOI structure.

Moreover, the Litwin patent, the Chiang patent, and the Tsang patent do not suggest making a varactor so that alternating P- wells and N+ regions are formed in a silicon layer of an SOI structure such that each of the P- wells and the N+ regions extends completely through the silicon layer to an insulation layer of the SOI structure. One of the advantages of such a varactor is improved tuning range over the varactors disclosed in the Litwin and Chang patents. This advantage is not suggested by the cited references.

Therefore, independent claim 32 is patentable over the Litwin patent, the Chiang patent, and/or the Tsang patent. Because independent claim 32 is patentable over the Litwin patent, the Chiang patent, and/or the Tsang patent, dependent claims 33-39 are likewise

patentable over the Litwin patent, the Chiang patent,  
and/or the Tsang patent.

**CONCLUSION**

In view of the above, the claims of the present application are definite and patentably distinguish over the art applied by the Examiner. Accordingly, allowance of these claims and issuance of the present application are respectfully requested.

Respectfully submitted,

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June 29, 2004